Design of High Speed Master-Slave D-type Flip-Flop in InP DHBT Technology

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Abstract — **In this paper we present design problems of high speed master-slave D-type flip-flop (MS D-FF). Essential to the long haul optical fiber communication systems, this circuit is critical since it operates at the highest clock frequency for a given bit rate. We discuss specific aspects of electrical design of such a circuit and underline some important points of layout of Gigabit circuits. The MS D-FF was fabricated in our self-aligned InP DHBT technology. On wafer measurements show correct operation at 40 Gb/s.**

I. Introduction

The important increase of communication services, and particularly the internet traffic, needs to be supported by the development of adequate networks. Optical fiber, with its huge transmission capacities, is the dominant technology for long haul communications.

To achieve high speed transmissions, several data tributaries have to be combined together. Time Division Multiplex (TDM) assigns individual data channels to time slots in a higher speed stream. As the number of multiplexed channels increases, the bit period get shorter. Systems with 10 Gb/s (corresponding to SDH STM-64 European standard and SONET OC-192 North American standard) are now in commercial use. Due to the hierarchical nature of these standards, with multiplication by four of the transmission bit-rate when passing to the next level, the next single channel to be implemented is 40 Gb/s. Progress in high-speed microelectronics has already permitted to set up 40 Gb/s Electrical TDM (ETDM) experiments, while first 80 Gb/s circuits start to be evaluated.

A combination of ETDM and Dense Wavelength Division Multiplex (DWDM) results in multi-Terabit transmission capacities. E.g., in [1] 5 Tbit/s transmission consisting in the combination of 125 wavelengths at 42.7 Gb/s each over 12x100 km has been reported.

Different Very High Speed ICs (VHSICs) are necessary to realize ETDM systems. Each of them presents specific requirements and is a challenging design task at 40-80 Gb/s.

In this communication we present the design problems both at electrical and layout level and realized tradeoffs for D-FF decision circuit. The difficulty of this circuit, compared to other composing the ETDM systems, consists in its high clock rate. In fact it operates at the clock rate equal to the bit rate in contrast with MUX and DMUX circuits which operate at half the clock frequency. D-FF and decision circuits have been fabricated in different technologies: GaAs HBT [2], InP HBT [3-4], InP HEMT [5].

In this paper we present the design of D-FF circuits with particular focus on electrical level optimization and layout aspects. This circuit was fabricated in InP DHBT technology and measured at 40 Gb/s (measurement setup limitations).

This communication is organized as follows. In section II, we briefly present the InP HBT technology used for circuit fabrication. In section III we discuss various aspects of circuit design followed by section IV devoted to layout problems. Finally experimental results are shown in section V.

II. Technology

The circuit we present has been fabricated in an InP DHBT technology, developed within OPTO+. The base line technology has been presented in detail in [6-7]. Unity current gain cut-off frequency, F_t, of 160 GHz and a corresponding maximum oscillation frequency, F_{max}, of 220 GHz have been measured for 1.5 µm emitter width transistors at 1mA/µm² current density.

The InP/InGaAs self-aligned transistors have been fabricated on CBE-grown epitaxial structure. The use of a graded base eases the HBT scaling and permits emitter width reduction without current-gain degradation. A high breakdown voltage (BV_{CE0} >7 V) is the result of the double heterojunction structure.

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In order to improve the frequency characteristics of the devices it is important to minimize both the base resistance R_B and the base-collector junction capacitance C_{BC}. The general approach consists in decreasing the dimensions, but then parasitic effects tend to dominate. For emitter lengths smaller than 10 µm, a self-aligned base-pad isolation process has been introduced. It reduces the parasitic base-collector effects. Thus, high performances can be maintained even for small transistor length: F_t above 150 GHz is achieved for currents in the 2-6 mA range, for 1.5 x 2 μm^2 devices. Such kind of transistors can be suitably used for very low power high frequency applications.

Three Ti/Au interconnection levels, TaN resistors, MIM capacitors and spiral inductors are available to realize the circuit layout.

III. Circuit Design

D-type flip-flop (D-FF) is a key electronic component in transmission systems. It is used to synchronize and/or delay data to the clock, but also as a reshaper and, at the receiving end, as a decision circuit. This decision circuit is at the core of demultiplexing circuits, which can be realized (at the expense of phase margin and SNR) with two D-FF operating at half the bit-rate, with clock and clock-bar. It can also be used for more complex functions, such as eye-diagram monitoring [8].

The precise specifications of the D-FF depend on its role in the system. When used as a re-timer/re-shaper, jitter, rise and fall time are more important than sensitivity. At the receiving end, sensitivity is a key parameter, for its consequences in system design. For the eye-diagram monitoring, phase margin and sensitivity are the more important parameters.

A. Architecture

The MS D-FF circuit consists of an input buffer which is decisive for the sensitivity, the circuit core which realizes the D-FF function and an output buffer. CML, ECL and E^2CL gates are used in different circuit parts depending on the function to be performed.

B. Design Optimization

Transistors sizing: As for all VHSICs, the design of the D-FF circuit is full custom. Individual transistor geometries have to be adjusted to reach optimal circuit performances. The base resistance R_b and base collector capacitance C_{BC} play a leading role in the propagation delay time, thus, it is necessary to lower the $R_b \times C_{BC}$ product. This can be done by choosing the smallest emitter width allowed by the technology and providing the appropriate current density in the transistor.

In our design, transistors with emitter dimensions 10x2 μm^2 were used. At 1mA/μm^2 current density, these transistors have F_t=140 GHz and F_{max}=150 GHz.

Electrical simulations: Precise time domain simulations are necessary to assess correct operation of VHSICs. Pseudo-random source is representing the input signal and lengthy transient simulations are realized to evaluate the time jitter. A simulator from the SPICE family has been used. To represent InP HBT, the non linear Gummel Poon model [9] has been used with corrections due to the specific behavior of III-V HBT technology [10]. In fact, although it is difficult to represent different phenomena of InP HBT behavior with this model, the careful modeling in large domain of bias currents allows to predict both static and dynamic behavior of the transistors.

Emitter-follower (EF) optimization: To achieve a correct operation at the highest possible speed, ECL or E^2CL architectures are used. The EF structures allow to obtain better matching between CML stages. However these structures, especially realized with rapid transistors must be carefully designed to avoid excessive ringing. These oscillations are caused by the combination of a negative real part of EF impedance and input capacitance. The damping techniques with resistors can be used but at the expense of increasing the rise/fall time. The availability of precise transistor models is crucial for optimization of this stage. In fact, different τ and C_{BC} combinations can model similar transistor behavior, while leading to completely different effect on oscillations.

IV. Layout Problems

As the complexity and the circuit speed increase, the performances are limited by the parasitic elements introduced during the layout process, like crossing capacitances, imperfect ground references, long transmission lines, etc. [11-12]. Qualitative rules are applied to reduce the degradation due to these parasitic elements: crossing areas between the interconnection levels are minimized and inductive voltage-supply metallization avoided as far as possible. Due to circuit complexity it is not possible to maximally shorten all connections. For a given circuit architecture, critical connections are identified and shortened as much as possible.

Furthermore, full-custom layout techniques (symmetrization, parasitic extraction) were developed and utilized throughout the design.

A. Layout parasitic extraction

In-house developed layout extraction tool [13] has been used in order to simulate the most critical layout parasitic effects. This tool permits the extraction and the post-simulation of each interconnection line (coplanar or microstrip) which is considered as critical. However, the complexity of this layout does not allow the simulation of the circuit with all parasitic elements simultaneously taken into account.

B. Influence of parasitics in EF connection

In this section, we show how degradation caused by neglected ground metallization parasitics can become dominating and have disastrous effects upon the circuit performance.

The first version of the D-FF circuit was simulated taking into account the crossing capacitances and interconnections considered as critical (Fig. 1a). As mentioned before, it is not possible to systematically take into account all parasitic elements. In our case, one of the connections (EF pair at the clock input connection to ground shown in Fig. 2) was badly dimensioned. The metallization was not large enough. The parasitic inductance of this interconnection caused voltage fluctuations resulting in closing the eye-diagram above 30 Gb/s. This effect was confirmed by simulation as presented in Fig. 1(b).

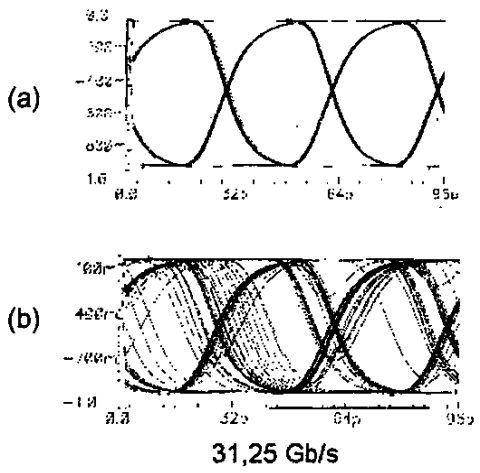

Fig. 1 D-FF simulation at 31.25 Gb/s (bit time = 32 ps)
(a) with main parasitics
(b) with main parasitics and EF connection to ground

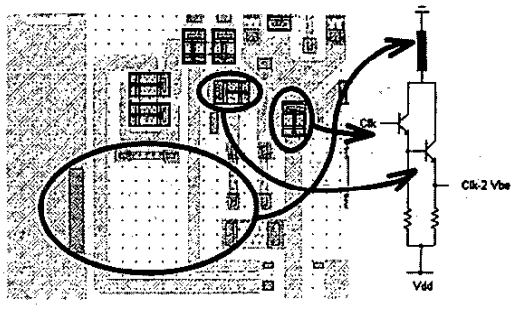

Fig. 2 Badly dimensioned EF connection to ground

This example shows the importance of the layout phase and the necessity of human expertise to properly choose the critical parts to be back-annotated for simulation, as the automated full parasitic extraction is presently not possible for VHSICs.

The layout was corrected and the microphotograph of the fabricated chip is shown in Fig. 3. The chip dimensions are 1.4×1.2 mm², and it is composed by 125 devices.

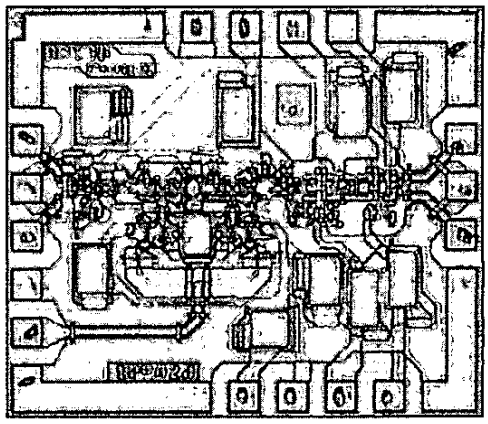

Fig. 3 Microphotograph of modified D-FF layout

V. Experimental Results

The measurement setup is composed as follows. A 20 Gb/s pseudo-random bit-pattern generator (PRBG) and its complementary are available. One data stream is delayed and is multiplexed with the other using a 40 Gb/s MUX. The PRBG and the MUX are clocked by the same frequency synthesizer. This synthesizer is synchronized with a low phase noise frequency synthesizer which provides the circuit's clock signal. A 50-GHz-sampling oscilloscope is used.

50 Ω on-chip output and input resistances provide an efficient impedance matching for testing and packaging. Less than –12 dB of signal reflection at the input and less than –8 dB at the output were measured up to 65 GHz (cf. Fig. 4).

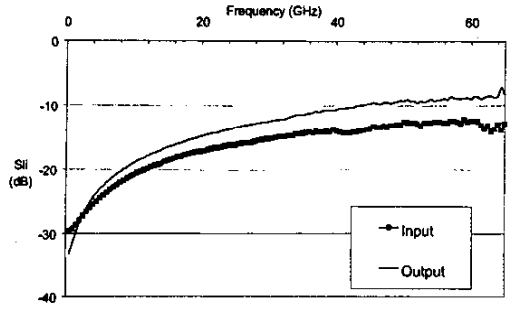

Fig. 4 Signal reflection measurement at the input and the output of the D-FF circuit

Measurement results are shown in Fig.5. A section of the input pulse sequence and the corresponding output at a data rate of 40 Gb/s are presented. High and low levels are correctly attained. The rise and fall times (20 to 80 %) are about 10 ps.

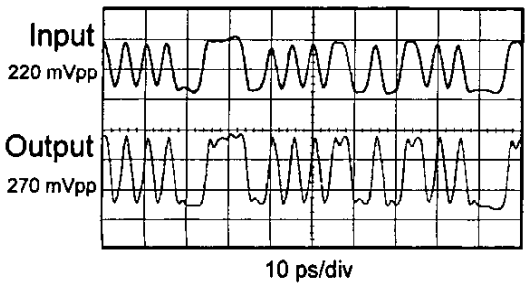

Fig. 5 Input and output pulse sequence at 40 Gb/s

The phase margin (PM) is 8 ps at 40 Gb/s which corresponds to 192° if we take into account the input data jitter (about 10 ps) as in (1).

$$\text{PM}\,[\text{deg}] = \frac{\text{Measured PM}}{\text{Bit duration} - \text{Input data jitter}} \times 360 \qquad (1)$$

V. Conclusion

We presented problems related to the design of high speed D-FF circuits. In particular, we discussed the problem of ringing which can appear in EF structures using rapid transistors necessary for high speed operation. We pointed out also some difficulties of circuit layout, and especially certain connections which can cause serious dysfunction of the circuit. A MS D-FF have been fabricated in InP HBT technology. The circuit operates correctly at 40 Gb/s.

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